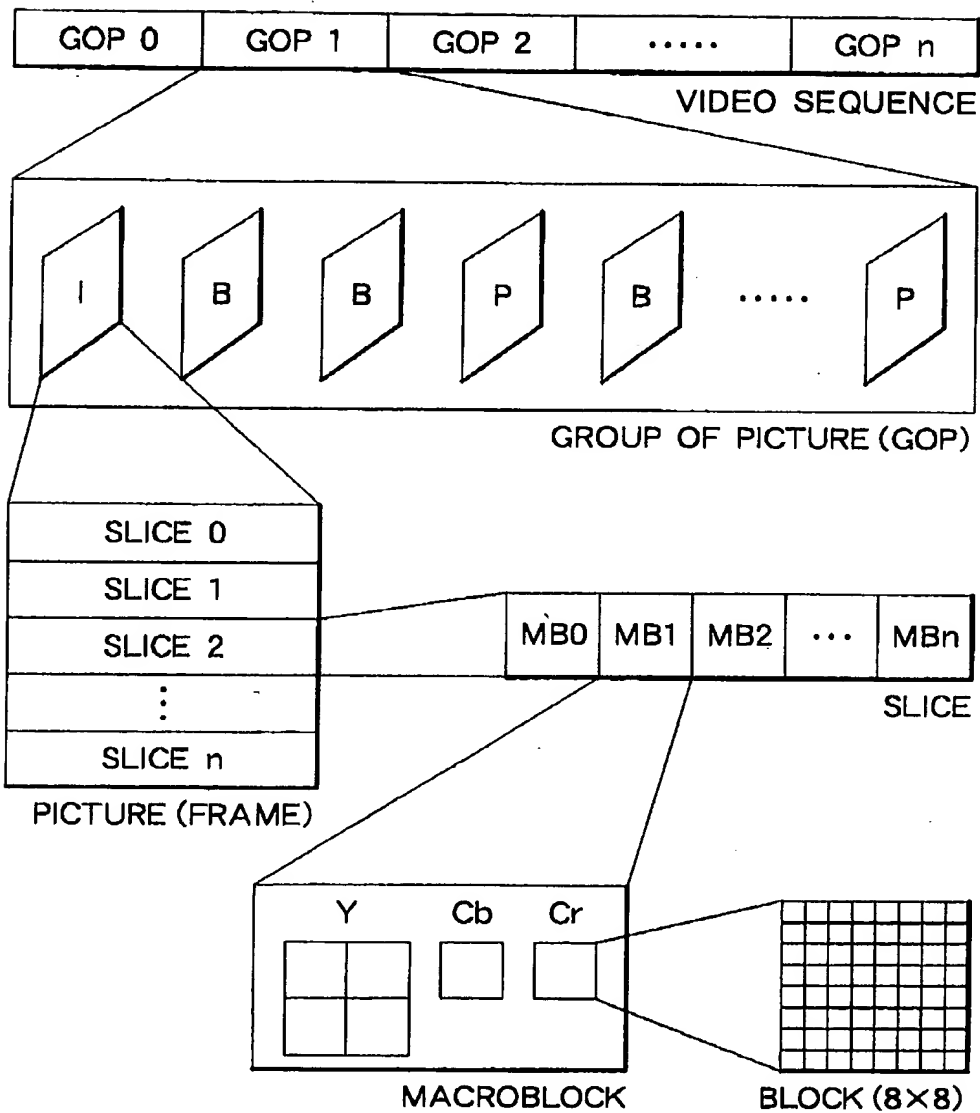


FIG. 1





**FIG. 3**

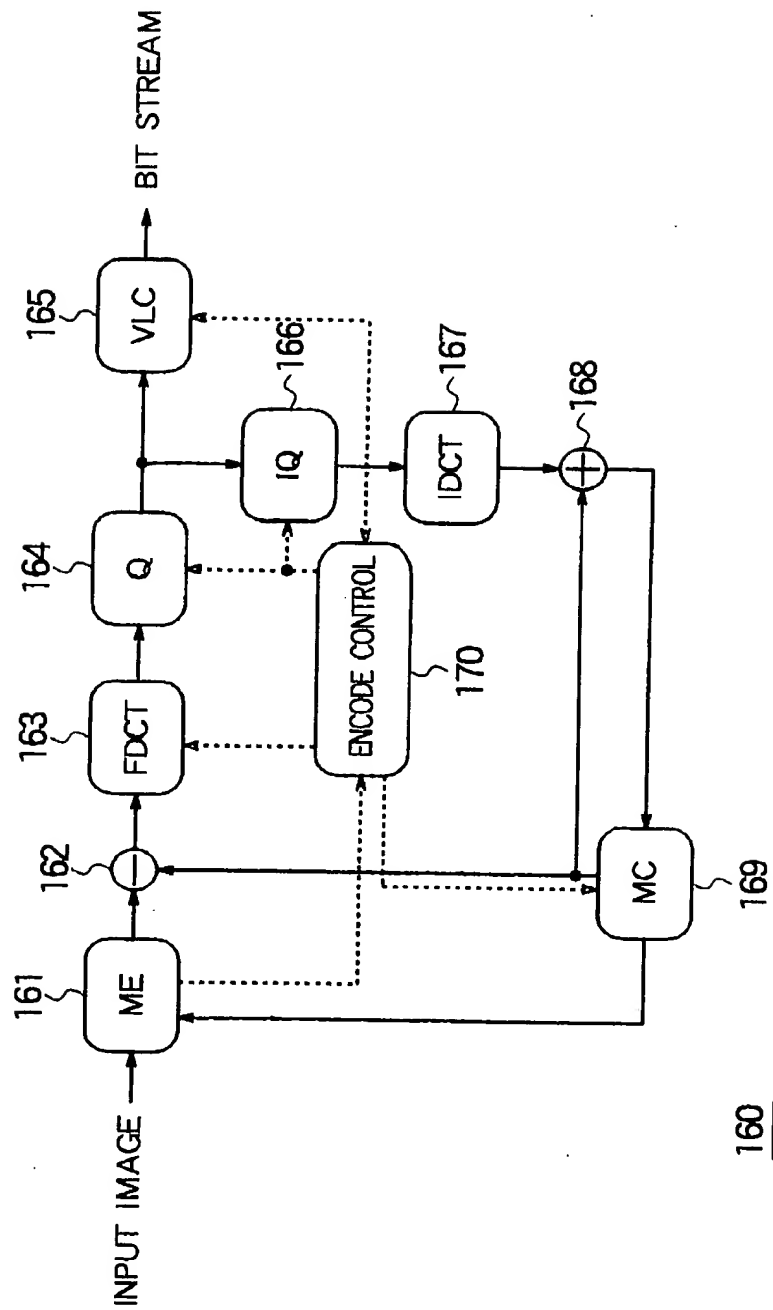


FIG. 4

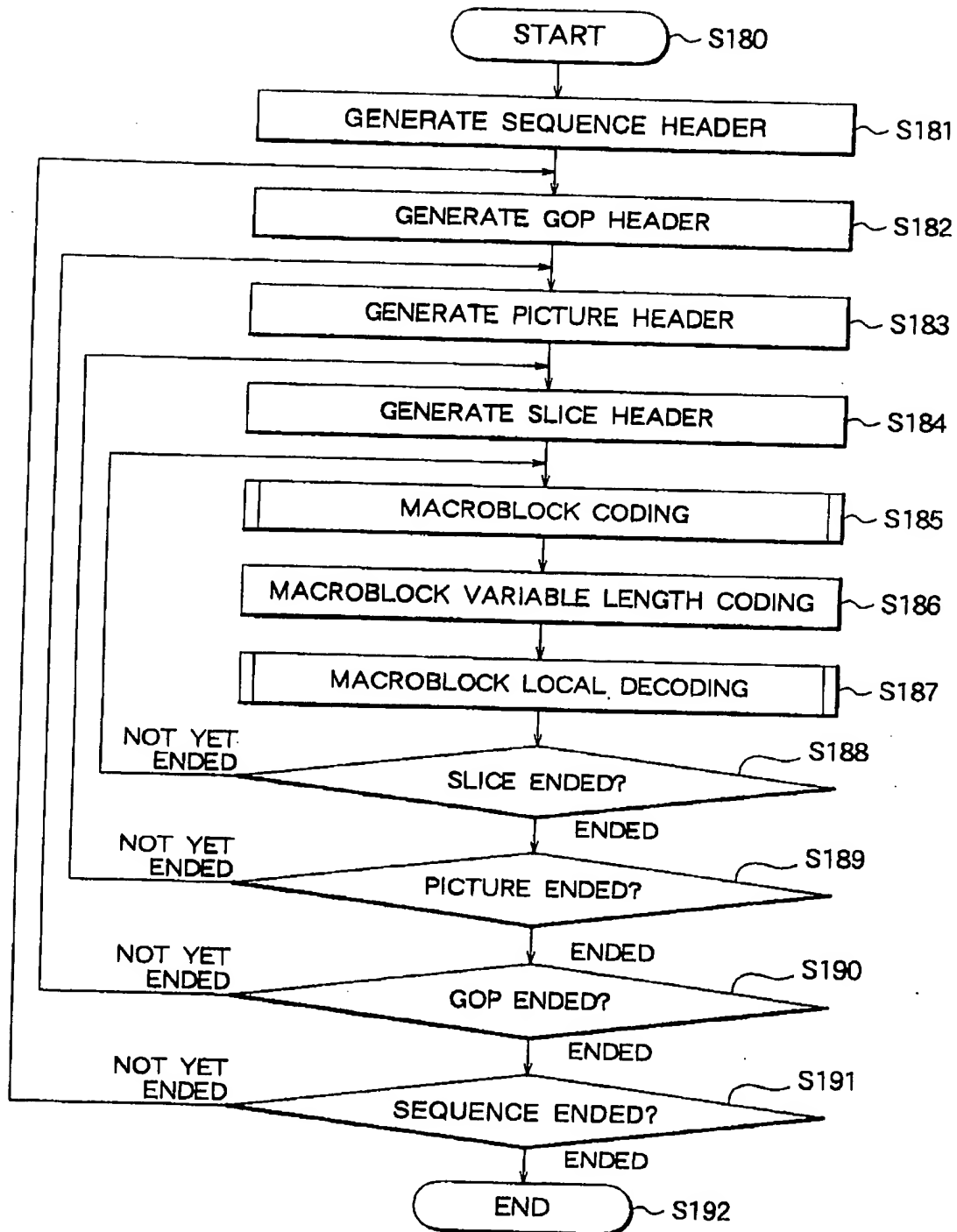


FIG. 5

FIG. 5

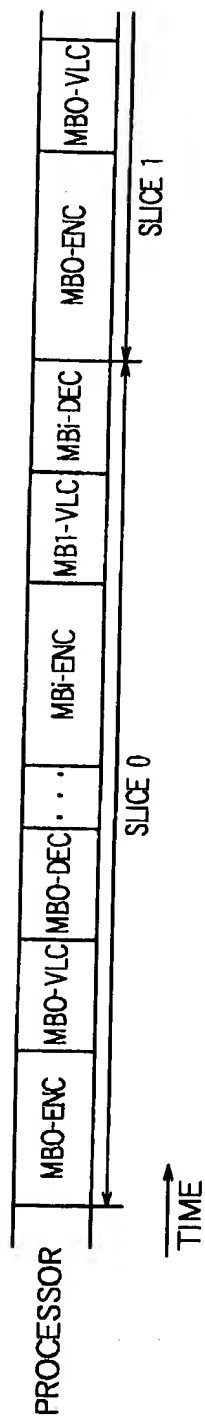


FIG. 6

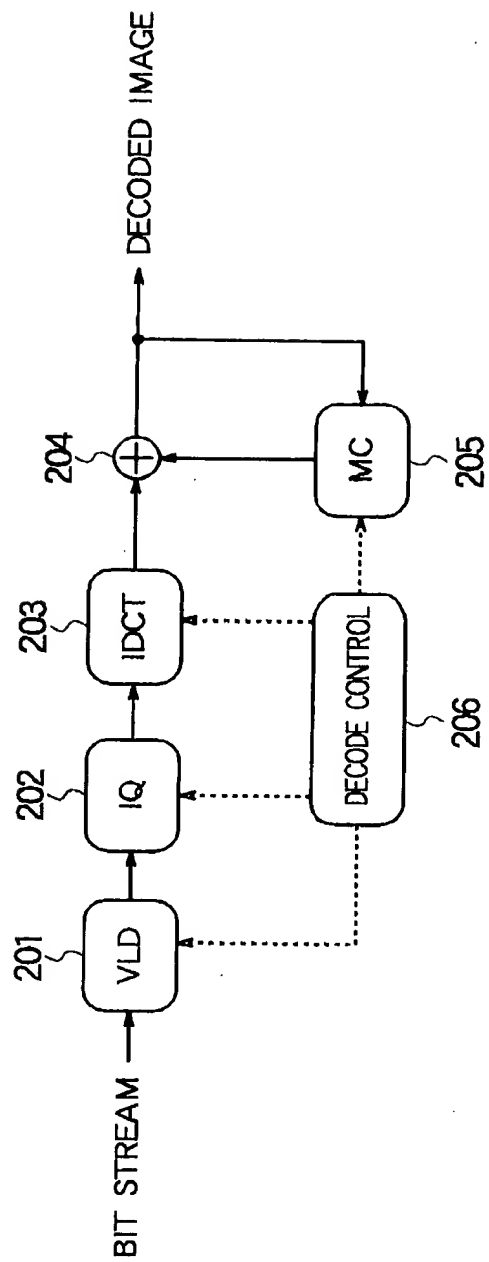


FIG. 7

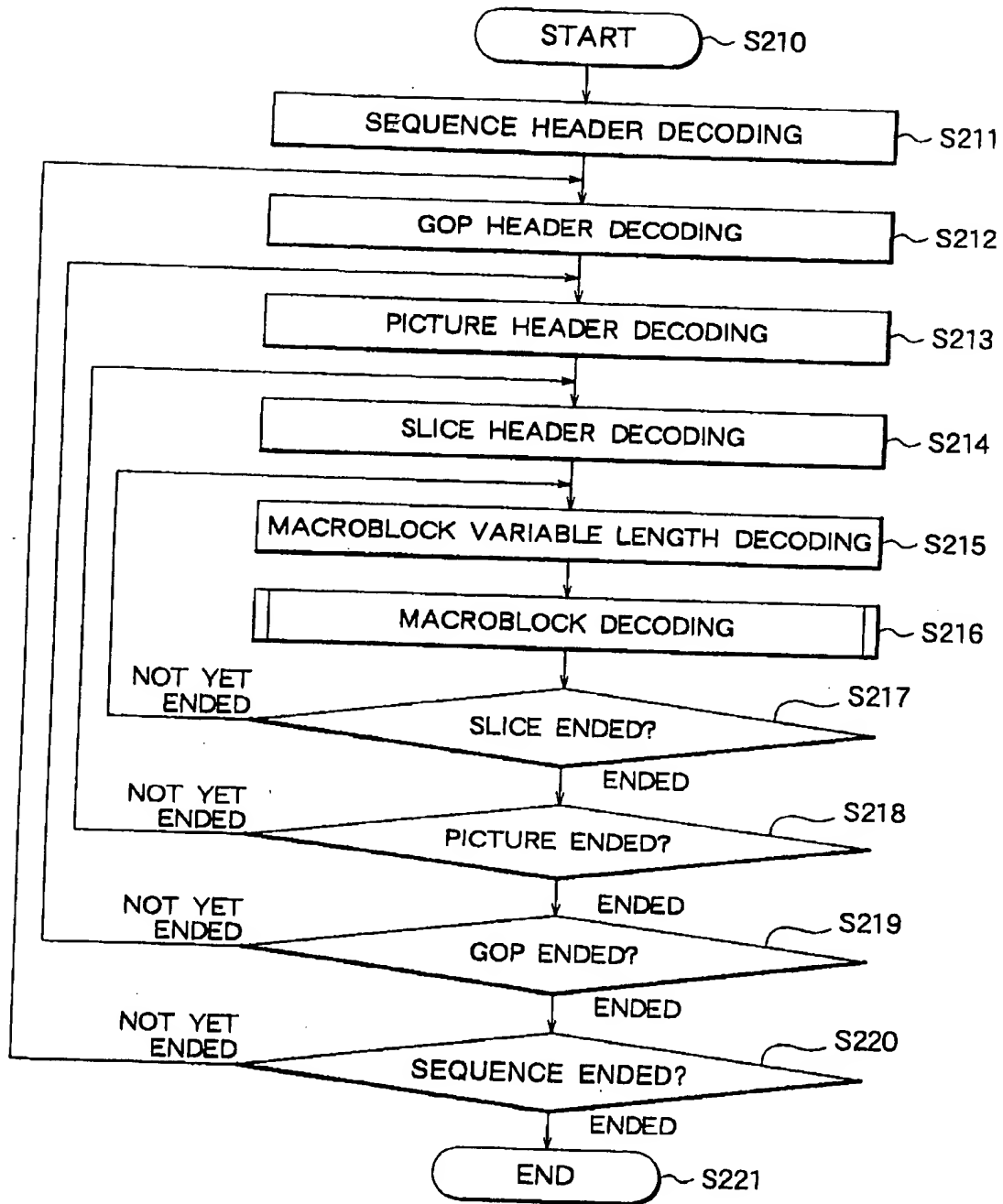


FIG. 8

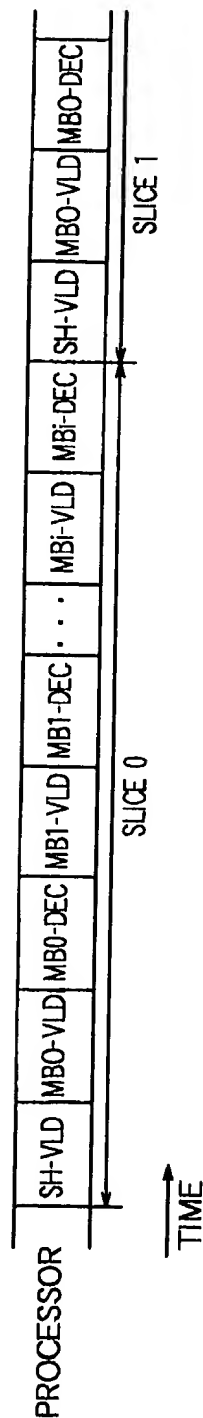
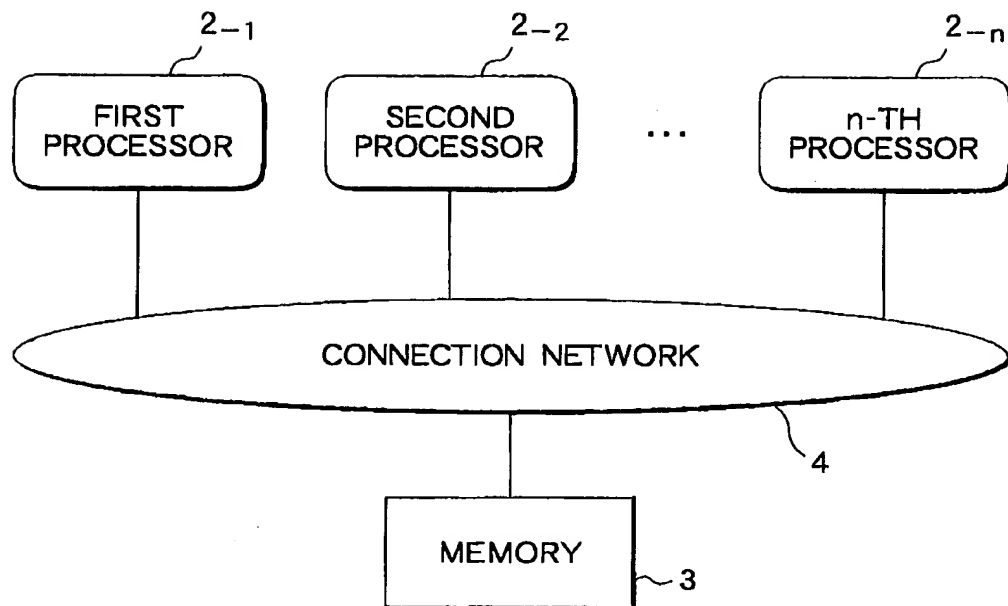




FIG. 9



# FIG. 10

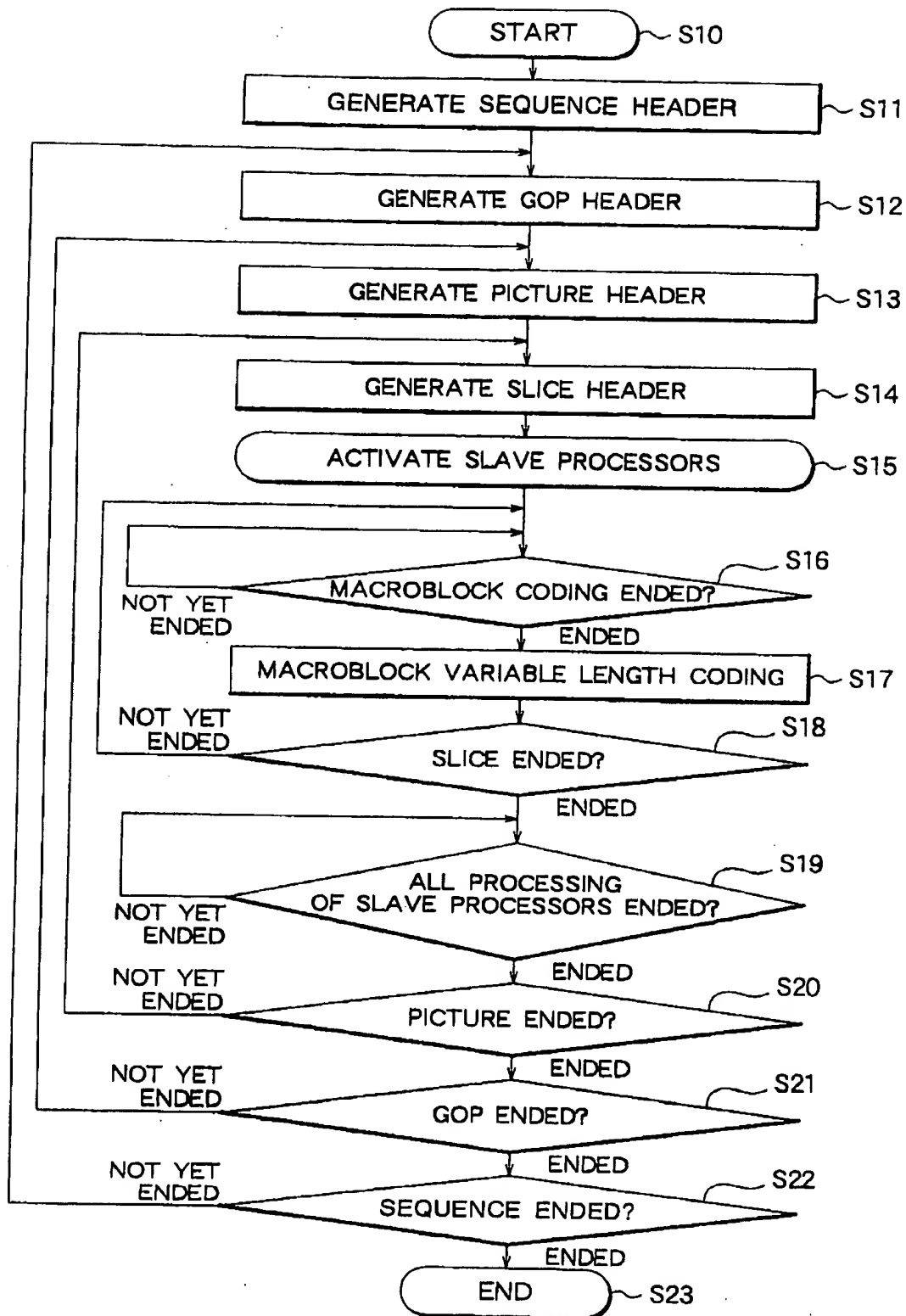


FIG. 11

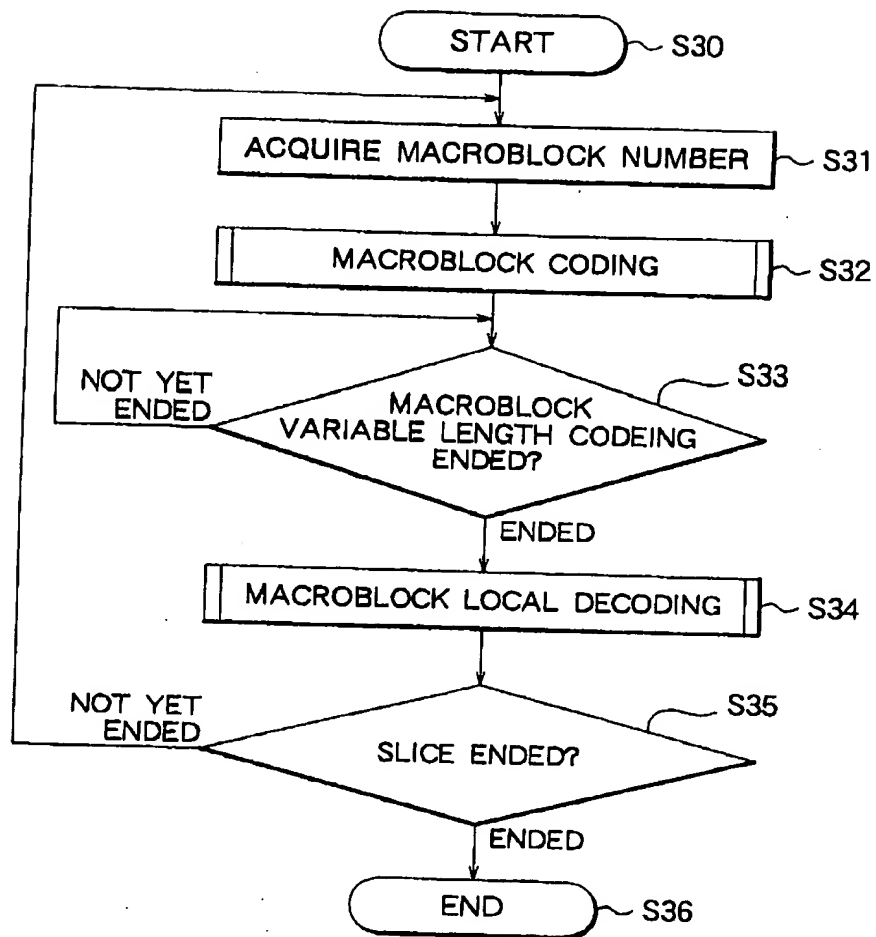


FIG. 12

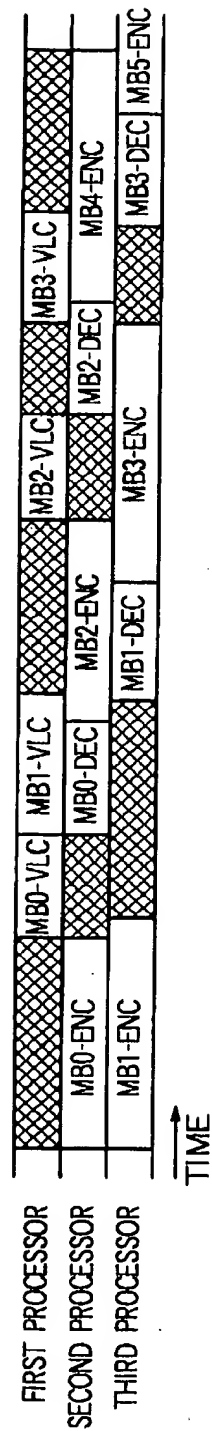


FIG. 13

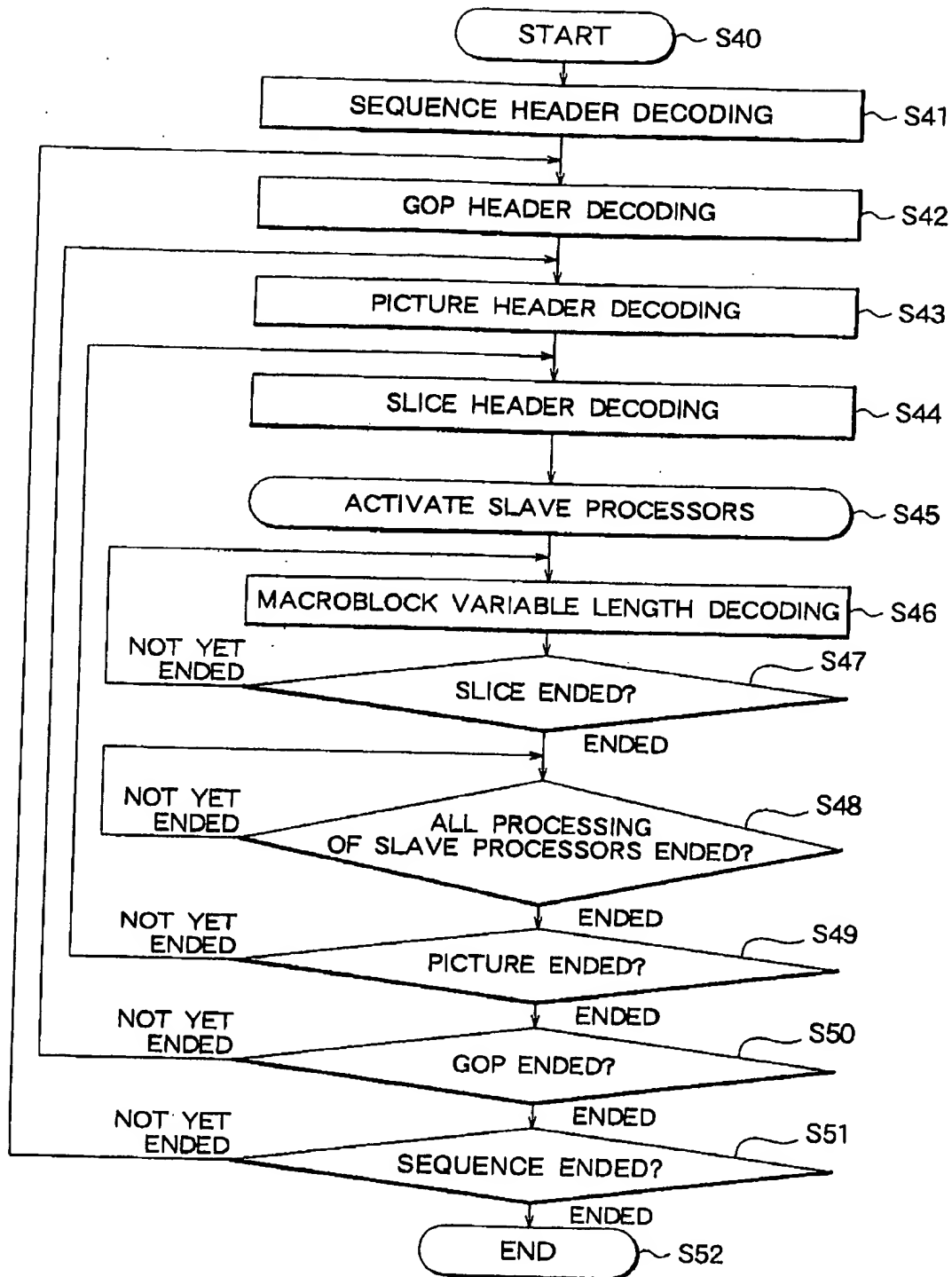
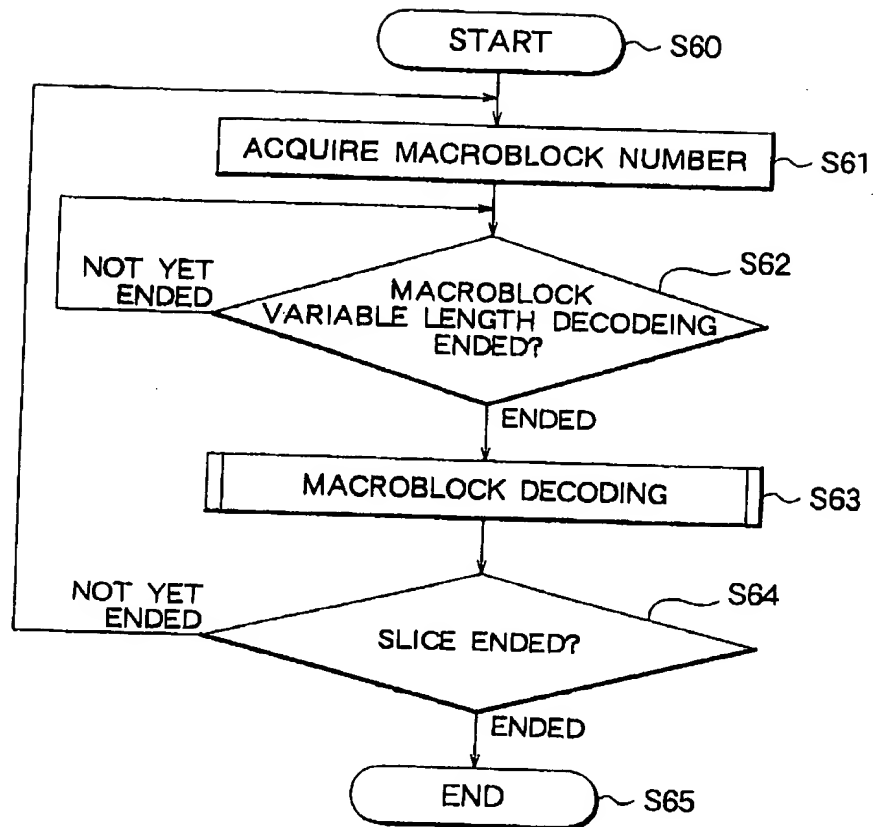


FIG. 14





# FIG. 16

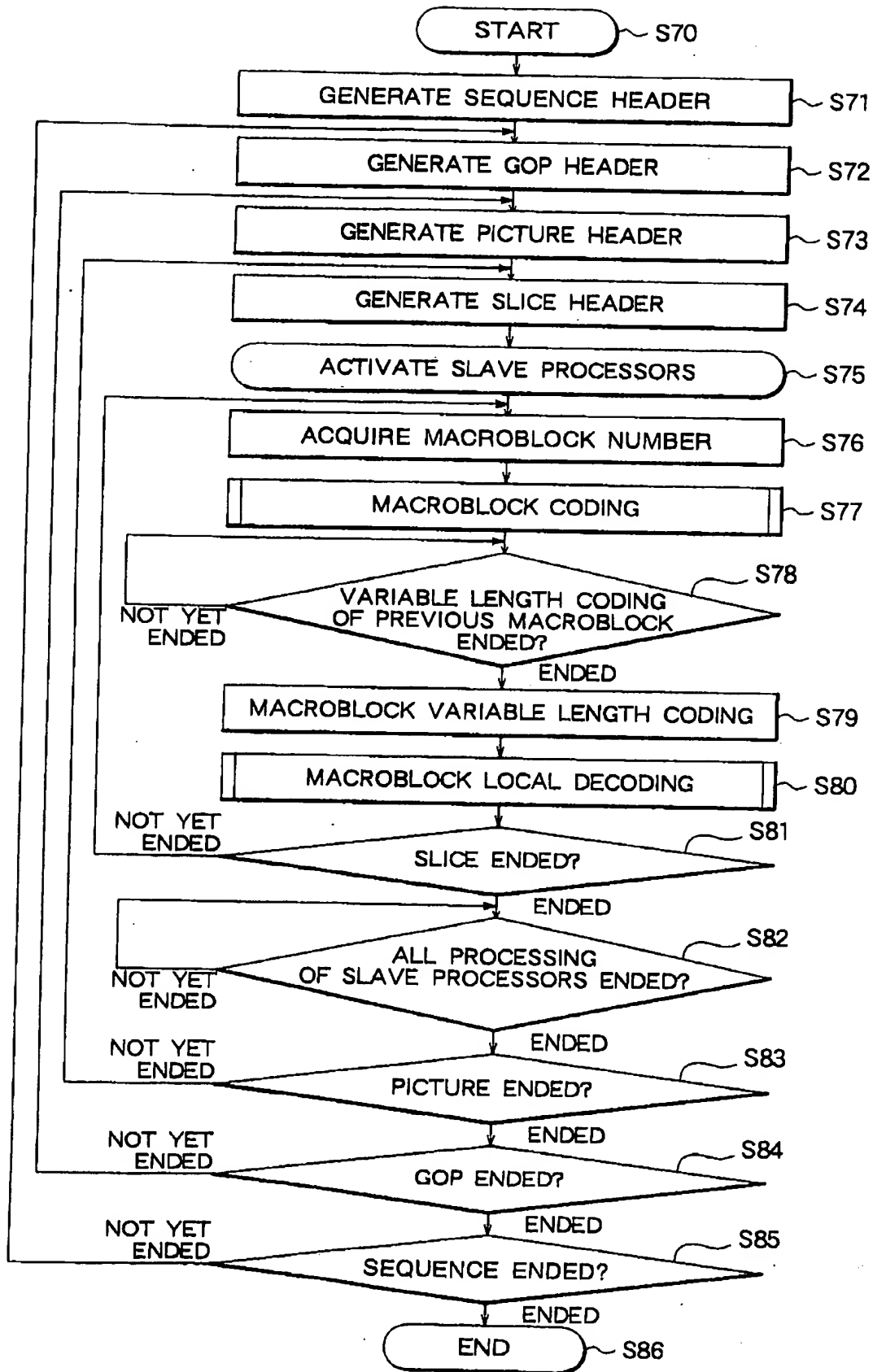




FIG. 17

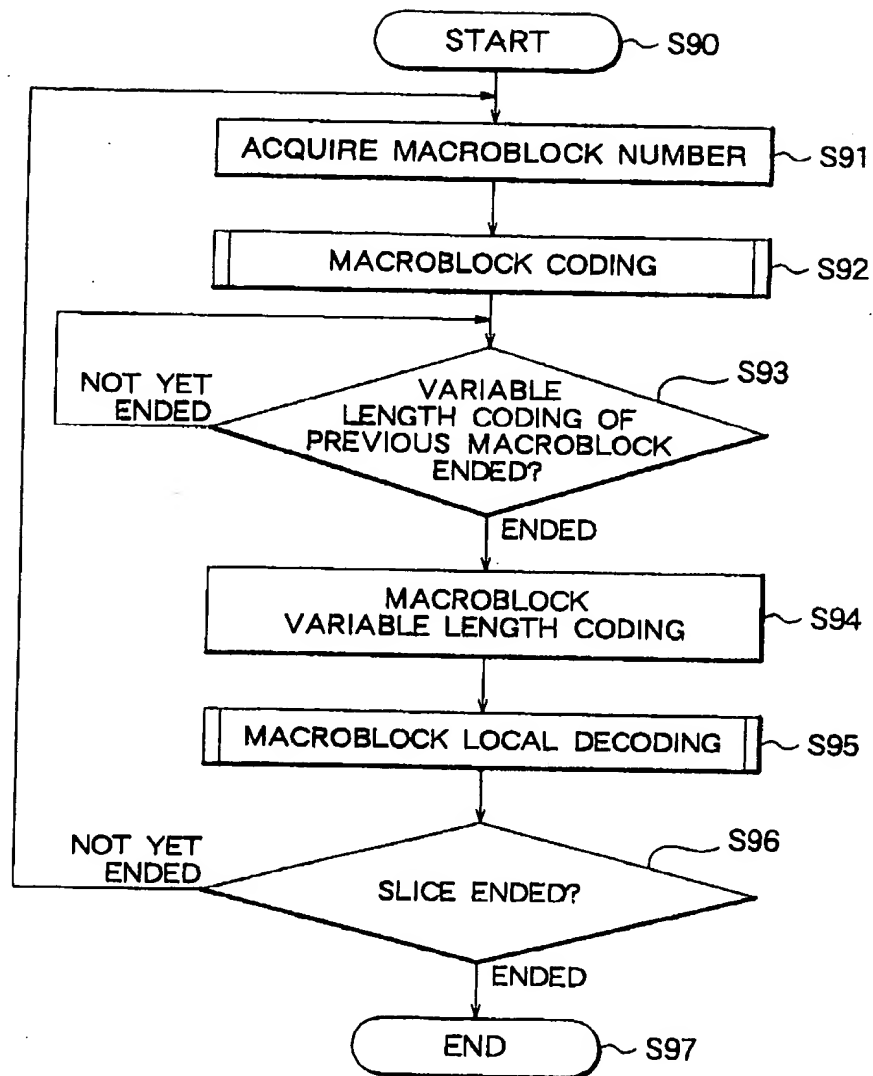


FIG. 18

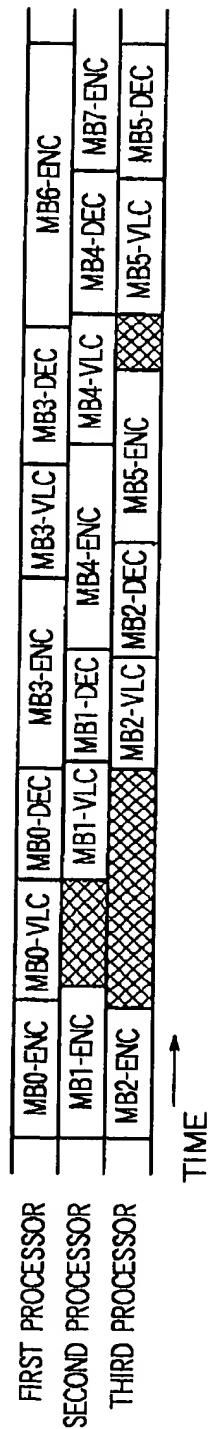


FIG. 19

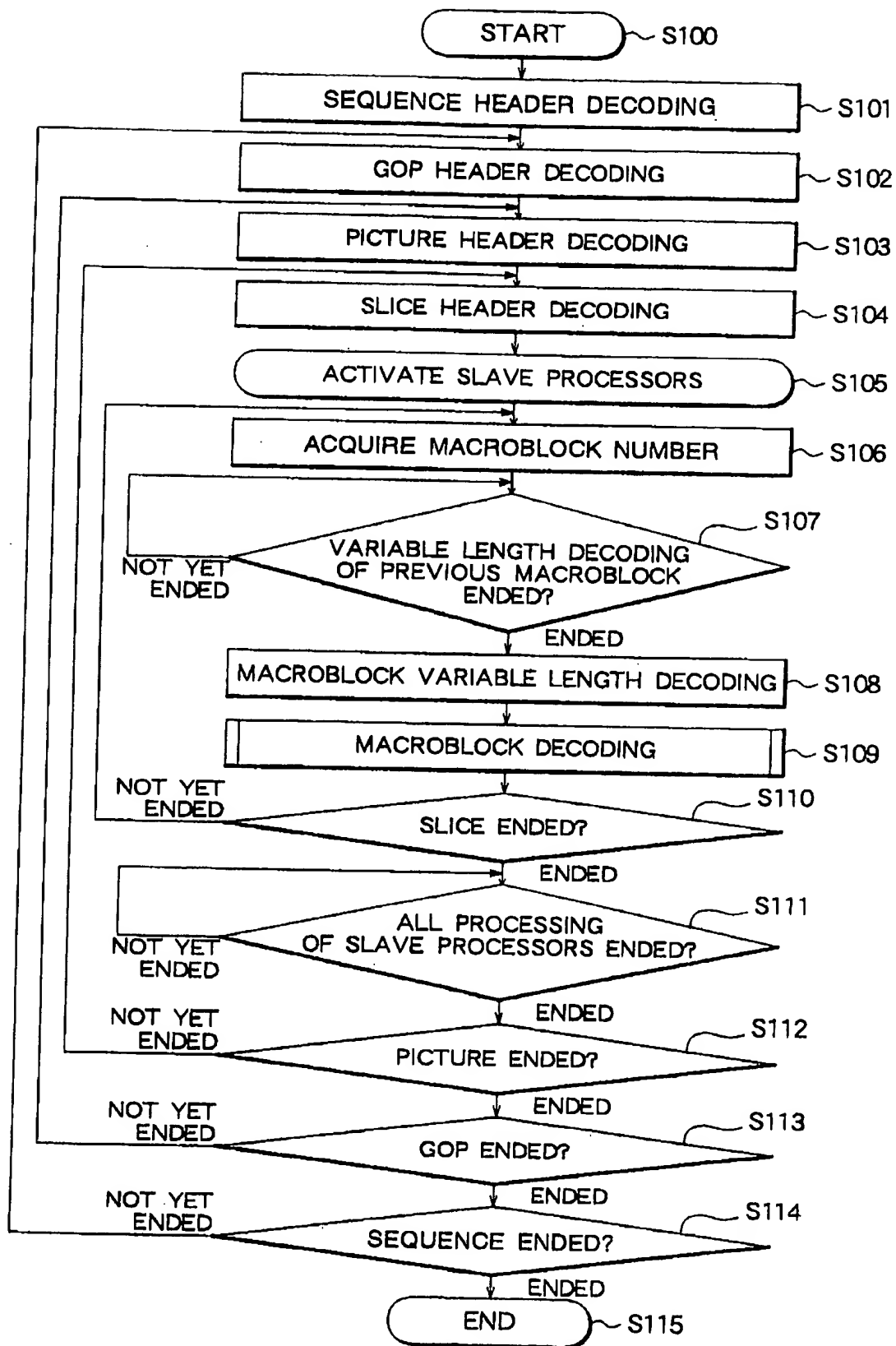


FIG. 20

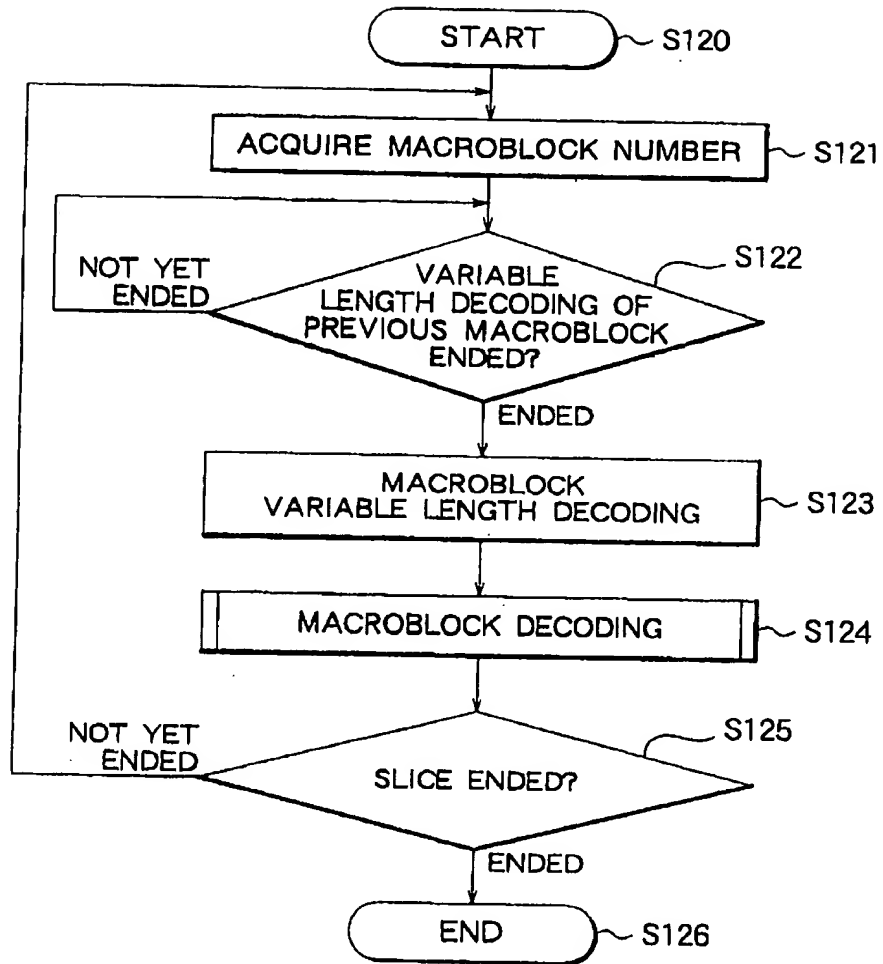


FIG. 21

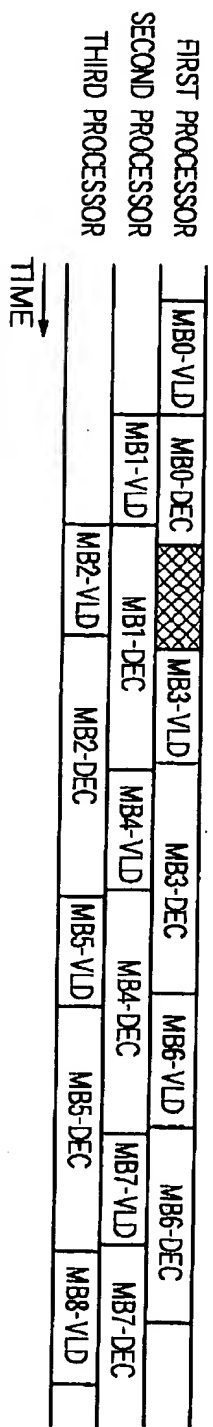


FIG. 21 is a timing diagram showing the sequence of operations for the three processors. The diagram illustrates the timing of the VLD (Valid) and DEC (Decoded) signals for the first, second, and third processors. The signals are shown as rectangular pulses, indicating the duration of each operation. The timing diagram shows that the first processor starts with MB0-VLD, followed by MB0-DEC, MB3-VLD, MB3-DEC, MB6-VLD, and MB6-DEC. The second processor starts with MB1-VLD, followed by MB1-DEC, MB4-VLD, MB4-DEC, MB7-VLD, and MB7-DEC. The third processor starts with MB2-VLD, followed by MB2-DEC, MB5-VLD, MB5-DEC, and MB8-VLD. The diagram also shows two shaded regions, indicating periods where the first and second processors are both active.